

METHOD FOR FABRICATING CAPACITOR IN SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

5 1. Field of the invention

The present invention relates to a method for fabricating a capacitor in a semiconductor device, and more particularly to a method for fabricating a capacitor which can prevent bridging of a storage node electrode by increasing bottom area of the storage node electrode and forming a prevention portion of the storage node on the bottom area.

2. Description of the Prior Art

15 As generally known in the art, a capacitor is an element that stores electric charges and supplies them to drive a semiconductor device, and it is generally known that size of unit cell has decreased and capacitance has increased to drive the semiconductor device by a little with the advance of high integration of the semiconductor device.

20 Although it has been necessary to minimize a capacitor with the advance of the high integration of a semiconductor device, limitations exist in storing electric charges, and it has been difficult to highly integrate the capacitors in

comparison with the size of the cell. Accordingly, structure for storing electric charges of a capacitor has been variously studied to settle the above problems occurring in minimization of the capacitor.

5 Method of utilizing substance with a high dielectric ratio, method of decreasing thickness of a dielectric substance, and method of increasing surface area of a capacitor, which is a primarily utilized method in recent years, etc., have been adapted to increase electric charges
10 of a capacitor.

Referring to structures of electric charge storing electrode in a capacitor, they can be largely divided into a stacking structure in which several layers are formed on small areas to obtain large area of a capacitor, a groove
15 structure in which grooves of desired depth are formed on a substrate of a semiconductor and a capacitor is formed on them thereby storing the electric charges thereon.

Specifically, the stacking structure includes fin type structure that is formed in a fin shape, a cylindrical type
20 structure that is formed in a cylinder shape, and a modified cavity type structure such as HSG (Hemispherical Shaped Grains) and Bellows, which is modified from a cavity type structure in order to increase capacitance of a capacitor.

However, when the method of utilizing substance of a big

dielectric ratio in order to increase storing capacity of electric charges in DRAM device of a semiconductor, limitations arise as a result of such substances with large dielectric ratio not being diversified. Accordingly, the capacity of storing electric charges depends on the sort of a certain substance being chosen.

Fig. 1 is a cross-sectional view for showing a method for forming a capacitor of a semiconductor device according to a prior art.

First, as shown in Fig. 1, a polysilicon layer 5 and a hard-mask layer 10 are sequentially stacked on a semiconductor substrate (not shown) having a desired lower structure, and etching is selectively performed on these layers to form gates G1 and an insulation spacer 2 at both sides of the gates G1.

Subsequently, a first polysilicon layer is formed on the substrate inclusive of the gates G1, and this layer is planarized to form plugs 15 that fill spaces made between the gates G1.

Then, a first interlayer insulation layer 20 is formed on the resultant substrate inclusive of the gates G1, and selective etching of this layer is performed to form a first contact hole (not shown) that exposes the plug 15, and a storage node electrode 25 filling the first contact hole is

formed.

Thereafter, a silicon nitride film 30 and a PSG (Phosphorous Silicate Glass) layer 32 are formed sequentially on the resultant substrate, and these layers are selectively
5 etched till an upper surface of the storage node plug 25 is exposed thereby forming a second contact hole 34.

Then, a polysilicon layer (not shown) for a storage node electrode is formed in the second contact hole 34 and is etched back, then the deepening-out of the PSG layer is
10 performed to obtain a cylindrical type storage node electrode 35 bridging the storage node plug 25.

Fig. 2 is a cross-sectional view of a process for showing problems occurring in the prior art.

However, as shown in Fig. 2, according to the above
15 prior art, when the cylindrical type storage node electrode has been formed and a cleaning process of the electrode has been performed, the storage node electrode is tilted to an adjacent storage node electrode, resulting in bridging defects between the storage node electrodes.

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SUMMARY OF THE INVENTION

Accordingly, the present invention has been made to solve the above-mentioned problems occurring in the prior

art, and an object of the present invention is to provide a method for fabricating a capacitor in a semiconductor device which can improve production yield by preventing tilt of the storage node electrode thereby resulting in the elimination
5 of the defects originated from a bridging phenomenon.

In order to accomplish this object, there is provided a method for fabricating a capacitor in a semiconductor device, the method comprising the steps of: forming an interlayer insulating film on a semiconductor substrate, which includes
10 a first contact hole exposing a certain portion of the substrate; forming a storage node plug filling the first contact hole; forming a first insulating film, a first silicon nitride film, and a second insulating film sequentially above the substrate inclusive of the storage
15 node plug; forming a second contact hole that exposes the storage node plug by removing the second insulating film, the first silicon nitride film, and the first insulating film partly; forming a recessed portion at side surfaces of the second contact hole by wet-etching the first insulating
20 film remained in the second contact hole; forming a storage node electrode of the capacitor, which is connected to the storage node plug, by filling the second contact hole inclusive of the recessed portion; removing the remained second insulating film; and forming a dielectric film and a

plate electrode sequentially on the entire surface of the storage node electrode structure.

Also, a step of forming a second silicon nitride film above the resultant substrate inclusive of the first contact
5 hole can be added, before forming the first insulating film.

Further, the first insulating film has etching rate faster than that of the first silicon nitride film, and comprises a BSPG film.

Moreover, the second insulating film comprises a PSG
10 film and is formed to a thickness of 10000 ~ 20000Å.

Also, the recessed portion of the storage node electrode has a broader width than that of any other portion of the storage node electrode.

15 BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the
20 accompanying drawings, in which:

Fig. 1 is a cross-sectional view showing a method for forming a capacitor of a semiconductor device according to a prior art;

Fig. 2 is a cross-sectional view for showing problems

originated from the prior art;

Figs. 3A through 3H are cross-sectional views showing each process of a method for fabricating a capacitor of a semiconductor device according to one embodiment of the present invention; and

Fig. 4 is a cross-sectional view showing process of the method for fabricating a semiconductor device according to another embodiment of the present invention.

10 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, preferred embodiments of the present invention will be described with reference to the accompanying drawings. In the following description and drawings, the same reference numerals are used to designate the same or similar components, and so repetition of the description on the same or similar components will be omitted.

Figs. 3A through 3H are cross-sectional views showing each process of a method for fabricating a capacitor of a semiconductor device according to one embodiment of the present invention.

First, as shown in Fig. 3A, a polysilicon layer 102 and a hard-mask layer 110 for forming gates are sequentially

stacked on a semiconductor substrate 110 having a certain lower structure and gates G2 are formed by masking etching, and then insulating spacers 104 are formed at both sides of the gates G2.

5 Subsequently, after forming a polysilicon layer (not shown) for plugs on the substrate inclusive of the gates G2, planarization of the layer is performed to form plugs 120 filling spaces made between the gates G2. In this process, although not shown in the drawing, the plugs 120 are
10 connected to impurity regions of source/drain below the substrate.

Then, an interlayer insulating film 140 is formed above the resultant substrate inclusive of the plugs 120, and the interlayer insulating film is selectively etched to form a
15 first contact hole (not shown) that exposes the plugs 120.

Thereafter, a polysilicon layer for a storage node contact is formed above the resultant substrate inclusive of the first contact hole, and it is planarized to form storage node plugs 160 filling the contact hole.

20 Referring to Fig. 3B, a first insulating film 180 is formed to a thickness of 500 ~ 1000 Å above the resultant substrate inclusive of the storage node plugs 160, and the first insulating film 180 has faster etching rate than that of a silicon nitride film 200 that works as a etching barrier

film at the time of following wet-cleaning. In this process, a BPSG film is adapted as the first insulating film 180.

Subsequently, the silicon nitride film 200 is formed above the first insulating film 180 to a thickness of 500 ~1000 Å. In this process, the silicon nitride film 200 is used as an etching barrier film at the following deepening-out process by means of the wet-cleaning.

Referring to Fig. 3C, a second insulating film 220 is formed above the silicon nitride film 200 to a thickness of 10000 ~ 20000 Å that is the same thickness of the desired storage node electrode. In this process, a PSG film is adapted as the second insulating film 220.

Then, a polysilicon layer 240 for a hard-mask is formed to a thickness of 2000 ~ 5000 Å above the second insulating film 220.

Referring now to Fig. 3D, a mask pattern (not shown) for making a storage node electrode is formed above the polysilicon layer 240 for making a hard-mask by using a photoresist (not shown), and the polysilicon layer 240 for the hard-mask is partly dry-etched by using the mask pattern.

Then, after the mask pattern for making the storage node electrode is removed, the second insulating film 220, the silicon nitride film 200, and the first insulating film 180 is dry-etched by using the polysilicon layer 240 for the

hard-mask remained after the etching as a barrier thereby forming a second contact holes 250 that expose the storage node plugs 160.

Referring now to Fig. 3E, a deepening-out process is performed above the resultant substrate by using wet-cleaning to partly etch side surfaces of the first insulating film 180 to thereby forming a recessed portion 180a in the insulating film 180.

Accordingly, the recessed portion of the storage node electrode has a broader width than that of any other portion of the storage node electrode. In this drawing, drawing numeral 251 refers to a second contact hole 251 formed after the completion of the wet-cleaning process.

Referring now to Fig. 3F, a doped or non-doped polysilicon layer (not shown) for a storage node is formed above entire resultant substrate to a thickness of 300 ~ 500 Å so that the second contact holes 251 made after the completion of the wet-cleaning process are filled.

Then, a CMP (Chemical Mechanical Polishing) process or etch-back process is performed to the resultant substrate in order to expose upper surface of the second insulating film 220 thereby separating the polysilicon layer for the storage node. In this drawing, drawing numeral 260 refers to a storage node electrode of a capacitor, which is connected to

the storage node plug 160.

Referring to Fig. 3G, a deepening-out process of the PSG layer 220 is performed by wet-cleaning.

In this process, the storage node electrode 260 becomes
5 to equip with wide bottom area (denoted by "A") to construct very stable shape thereby preventing tilting phenomenon occurred between the adjacent storage node electrodes. Further, surface area of the storage node electrode 260 is increased due to the wide bottom area thereof, thereby
10 increasing the capacitance at the time of making a following dielectric film.

Also, when a MPS (Metastable Phase Silicon) layer is grown on a surface of the storage node electrode 260, it can increase the surface area thereof, thereby increasing the
15 capacitance of the capacitor.

Referring now to Fig. 3H, a dielectric film 280 is formed on the surface of the storage node electrode 260 by using Ta_2O_5 or NO.

Then, a polysilicon layer 300 for a plate electrode is
20 formed above whole resultant substrate to cover the dielectric film 280 to a sufficient thickness by using any one selected from the group consisted of doped polysilicon, Ti, and TiN thereby completing the capacitor.

Fig. 4 is a cross-sectional view showing process of the

method for fabricating a semiconductor device according to another embodiment of the present invention.

As shown in Fig. 4, before forming the second interlayer insulating film 180 above the resultant substrate inclusive
5 of the polysilicon layer 160, a silicon nitride film is formed to a thickness of 300 ~ 1000 Å thereby using it as an etch barrier film in the wet-etching process.

As explained above, according to the method for fabricating a capacitor in a semiconductor device of the
10 present invention, tilting phenomenon of the storage node electrode in the integrated DRAM is prevented, thereby improving defects originated from the bridging of the electrodes and obtaining production yield increase.

Although a preferred embodiment of the present invention
15 has been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.